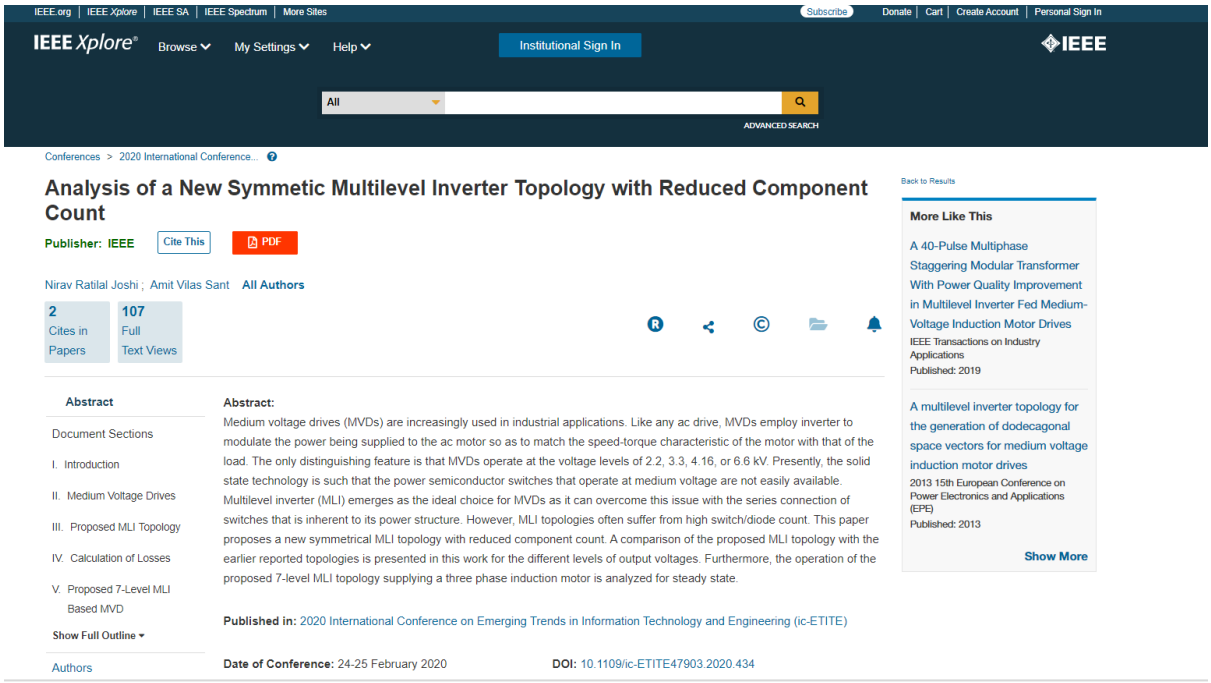
3.3.2 "Number of books and chapters in edited volumes/books published and papers published in national/ international conference proceedings per teacher during last five years

List of Research Papers Published by Faculty in the Calendar year 2020

Sl. No.	Name of the teacher	Title of the book/chapters published	Title of the paper	Title of the proceedings of the conference	Name of the conference	National / International	Calendar Year of publication	ISBN number of the proceeding	Affiliating Institute at the time of publication	Name of the publisher	Link to website of the Journal	Link to article / paper / abstract of the article
5	Prof. Nirav Joshi	**NA**	Analysis of a New Symmetic Multilevel Inverter Topology with Reduced Component Count	International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE)	-	**International**	2020	Electronic ISBN:978-1-7281-4142-8 USB ISBN:978-1-7281-4141-1 Print on Demand(PoD) ISBN:978-1-7281-4143-5	**Saffrony Institute of Technology**	Fast Track Publications	https://www.irjet.nett	https://www.irjet.net/archives/V6/i12/IRJET-V6I1292.pdf

Prof. Nirav Joshi

Analysis of a New Symmetic Multilevel Inverter Topology with Reduced Component Count



Analysis of a New Symmetic Multilevel Inverter Topology with Reduced Component Count

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***Abstract*— Medium voltage drives (MVDs) are increasingly used in industrial applications. Like any *ac* drive, MVDs employ inverter to modulate the power being supplied to the *ac* motor so as to match the speed–torque characteristic of the motor with that of the load. The only distinguishing feature is that MVDs operate at the voltage levels of 2.2, 3.3, 4.16, or 6.6 kV. Presently, the solid state technology is such that the power semiconductor switches that operate at medium voltage are not easily available. Multilevel inverter (MLI) emerges as the ideal choice for MVDs as it can overcome this issue with the series connection of switches that is inherent to its power structure. However, MLI topologies often suffer from high switch/diode count. This paper proposes a new symmetrical MLI topology with reduced component count. A comparison of the proposed MLI topology with the earlier reported topologies is presented in this work for the different levels of output voltages. Furthermore, the operation of the proposed 7–level MLI topology supplying a three phase induction motor is analyzed for steady state.**

Keywords*— *Induction motor drive, medium voltage drive, multilevel inverter, reduced switch multilevel inverter topology

I. Introduction

Globally, the industrial drives are the major consumers of electric energy. In USA, industrial drives consume about 60% to 65% of the generated electric power [1]. The industrial drives fed from medium voltage (MV) grids at 2.2, 3.3, 4.16 or 6.6 kV, [2], are termed as medium voltage drives (MVD). MVDs covers a wide power range, from 0.4 MW to almost 40 MW at the MV level of 2.3–13.8 kV. The high-power MVDs find wide applications in petrochemical and cement industries, water pumping stations, traction systems, steel rolling mills, etc [3]. Reference [4] has reported the installation of 1–4MW MVDs that operate at 3.3–6.6 kV.

Inverters are integral part of any *ac* drives and act as an interface to modulate power being delivered to the induction motors. With MVDs being deployed for the speed control of induction motors, they are a sub-set of *ac* drives. With the present state of solid state technology, power semiconductor switches operating at MV levels are not easily available. However, multi-level inverters (MLIs) involve series connection of multiple power semiconductor switches and are ideal power modulators for MVDs. References [5-8] have reported MLI based MVDs. Moreover, with the reduction in voltage total harmonic distortion (THD) at the output of MLI as compared to the 2–level inverter, the motor efficiency is further improved.

MLIs are *dc-ac* power converters that comprise of an array of power semiconductor switches to provide stepped *ac* voltages of the desired levels. As compared to the traditional 2–level inverter, MLI offers the benefits of lower distortion in output voltages, reduced *dv*/*dt* and voltage stress for power semiconductor switches, lower filtering requirements, ease of operation at higher voltage and power levels and reduced electromagnetic interference [9-12]. The three basic topologies of MLI are (i) Diode clamed or neutral point clamped (NPC) MLI, (ii) Flying capacitor (FC) or capacitor clamped MLI and (iii) Cascaded H-Bridge (CHB) MLI. Along with some emerging topologies of MLI, José Rodríguez et al have surveyed the basic topologies and presented a detailed analysis [2]. These topologies suffer from increase in switch or diode or capacitor count. The increased switch count necessitates increased gate drivers, protection units, which further adds to the system complexity and cost. Hence, there is a strong need for reduced switch MLI topology [13].

References [14-16] have presented different reduced switch MLI topologies. These inverter topologies are mainly classified as (i) symmetric reduced switch MLI, and (ii) asymmetric reduced switch MLI. In symmetric reduced switch MLI, values of all the *dc* sources are equal [13, 17-18]. Conversely, in asymmetric reduced switch MLI, the values of *dc* sources are unequal. Symmetric configuration of the MLI topology offers the benefits of good modularity and comparatively simple modulation and control. In [19], a modular MLI topology has been proposed wherein an H–bridge along with a bidirectional switch is used to produce 5–level single phase output waveform. Peng et al, in [20], have proposed a generalized MLI topology, wherein basic cells are employed to obtain multilevel stepped voltages. However, for 7–level unidirectional output voltage, the reported topology requires thirty switches.

This paper proposes a new symmetrical MLI topology with reduced switch count for MVD application. The paper proposes *n*–level multilevel inverter topology that has number of switches$(n + 7)/2$. Compared to the generalized MLI topology, for a single phase 7–level configuration, the proposed topology requires seven switches and six diodes, in which three switches generate zero, V_{dc}, $2V_{dc}$, and $3V_{dc}$ voltage levels. Additional four switches are required to generate bidirectional supply. However, the voltage balancing, explored in [20], is not included in this work. The operation of the proposed topology is compared with the three basic topologies and the topology reported in [20]. Moreover, the operation of proposed MLI topology with 7–level voltage output is analyzed for an MVD driving a 3–phase induction motor.

II. Medium Voltage Drives

MVDs are operated at medium voltage, 2.2, 3.3, 4.16 or 6.6 kV, to improve the motor efficiency. As the industrial drives are the major consumer of the total generated electric

power, a small save in the losses would lead to the major save in cost and energy. Fig. 1 shows the block diagram of an MVD comprising of a 3–phase induction motor fed from the utility through line side filter, 3–phase transformer, *ac-dc* converter, *dc* filter, *dc-ac* converter and motor side filter [3]. The line side and the motor side filters may or may not be employed depending on the system requirement and the selection of the converters. A phase shifting transformer at the grid side provides the prime benefit of the reduced distortion in the line current. *ac-dc* converter, connected at the secondary of the transformer, rectifies the *ac* voltage which is applied at the input of the *dc-ac* converter, also known as inverter. The *dc* filter connected between these two converters filters the ripple content in the *dc* supply being provided through rectification. The ON/OFF periods of the switches of the inverter are controlled to control the magnitude and frequency of *ac* supply being applied across the stator terminals. The voltage rating limitations of the commercially available power semiconductor switches was a key hindrance for MVDs. The need of higher current and voltage ratings, has led to the emergence of MLI fed induction motors in MVDs.

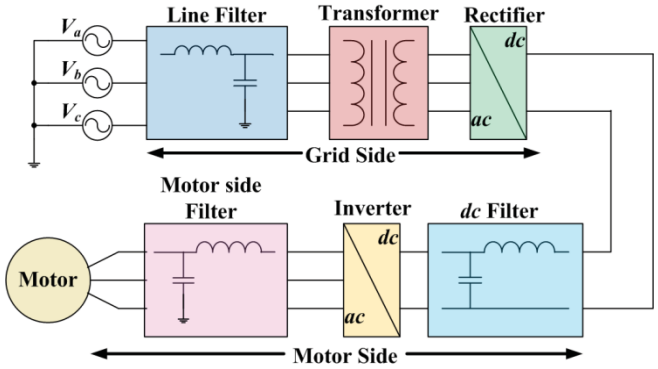

Fig. 1. Block diagram representation of MVD

III. Proposed MLI Topology

MLI provides the *dc-ac* conversion with stepped output voltage using multiple medium *dc* voltage sources at input that benefits in providing lower harmonic content in the output current. The three basic MLI topologies are: (i) CHB, (ii) NPC, and (iii) FC. Mainly, the need for decreasing the switch count has resulted in reduced switch count topologies, which can be classified as (a) Symmetrical reduced switch count topology and (b) Asymmetric reduced switch count topology. Symmetrical reduced switch count topology benefits in simple control technique and good modularity.

Fig. 2 shows the generalized MLI topology for *n*–level output voltage that reported in [20]. In this topology, for each voltage level a basic cell, made up of series connection of two IGBTs in parallel with a capacitor, is required. This topology is made up of Leg-1, Leg-2 and Leg-3 comprising of S_{p1}-S_{n1}, S_{p2}-S_{c1}-S_{c2}-S_{n2}, and S_{p3}-S_{c3}-S_{c4}-S_{c5}-S_{c6}-S_{n3}, respectively.

The proposed symmetric MLI topology is a modification of the generalized MLI topology in terms of reduced switch count and capacitor count for same number of levels in the output voltage. The proposed MLI topology for *n*–level output voltage is shown in the Fig. 3. This topology includes a string of *dc* sources, of equal magnitude V_{dc}, at the input. The number of *dc* voltage source is depends on the desired level in the output voltage. The number of *dc* voltage sources, N_s, for the proposed *n*–level MLI is given as,

$$N_s = (n-1)/2 \tag{1}$$

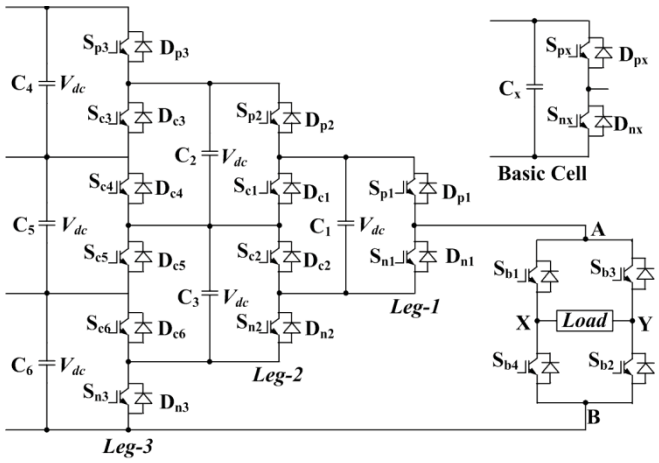

Fig. 2. 7–level generalized MLI topology for bidirectional stepped output voltage wavefrom

The power structure for the proposed MLI topology generates unidirectional stepped voltage waveform across the terminals A and B. An H–Bridge inverter, connected across the terminals A and B, facilitates the generation of bidirectional stepped voltage across the load terminals X and Y. Thus, the proposed MLI topology comprises of a power structure for generating a unidirectional stepped voltage waveforms and an H–Bridge inverter for converting the unidirectional stepped voltage into bidirectional stepped voltage. The switch count, $N_{sw,}$ and the diode count, N_D, for proposed *n*–level MLI topology is given as,

$$N_{sw} = (n+7)/2 \tag{2}$$

$$N_D = \sum_{i=0}^{\frac{n-3}{2}} \left(\frac{n-1}{2}\right) - i \tag{3}$$

The switches for producing *n*–level output voltage can be divided in two groups depending on its function.

Group: I Generates unidirectional staircase waveform with zero, V_{dc}, $2V_{dc}$, to $(n-1)/2 \times V_{dc}$ levels with the help of S_{p1}-S_{pn}.

Group: II Generates bidirectional voltage with zero, $\pm V_{dc}$, $\pm 2V_{dc}$ to $\pm (n-1)/2 \times V_{dc}$ levels with the help of S_{b1}-S_{b4}

Based on this, the *dc* voltage source, switch and diode count for the proposed MLI topology for 3, 5, 7 and 9 level output are stated in Table I. Also, this table presents a comparison of proposed MLI topology with CHB, FC, DC and generalized MLI topology, [20], for 3, 5, 7 and 9–level output voltage. The proposed MLI topology for 7–level output voltage consists of 7 switches where the conventional topologies consist of 12 switches and the generalized MLI topology incorporates of 16 switches for single phase 7–level bidirectional output voltage. From the comparison presented in Table I, it is clear that the proposed topology has least switch count for 3, 5, 7 and 9–level output voltage. Also, the proposed topology is superior in terms of reduced number of diodes and capacitor employed.

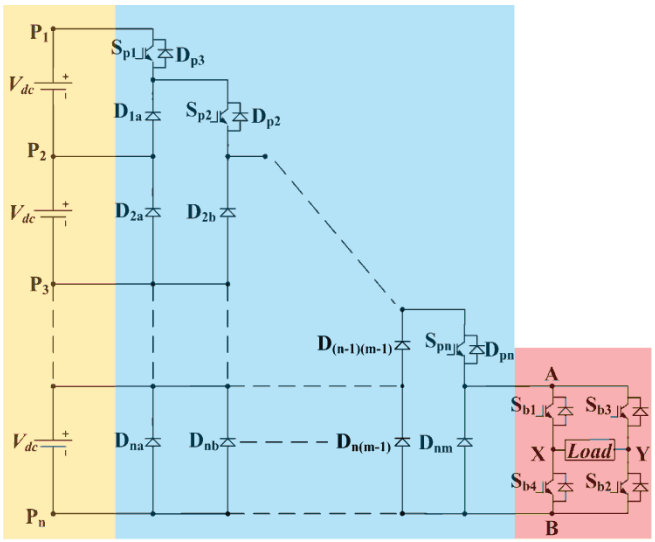

Fig. 3. Proposed MLI topology for *n*–level bidirectional stepped output voltage

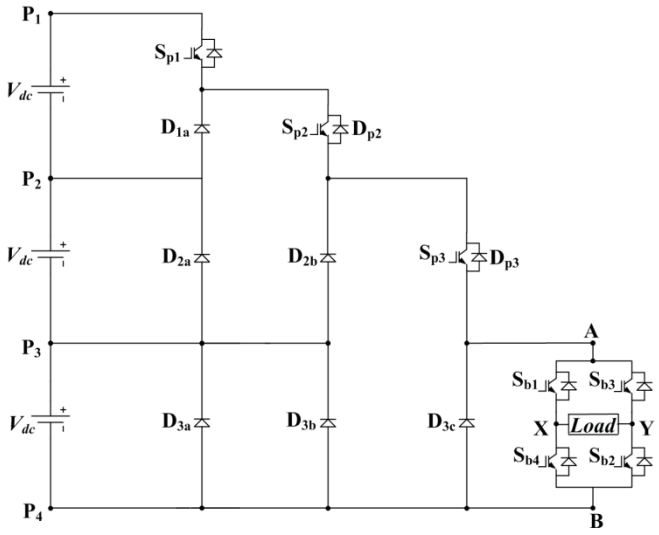

Fig. 4. Proposed MLI topology for 7–level bidirectional stepped output voltage

TABLE I. COMPARATIVE ANALYSIS OF COMPONENT COUNT OF DIFFERENT MLI TOPOLOGIES WITH PROPOSED MLI TOPOLOGY

Topologies→	CHB-MLI				FC-MLI				NPC-MLI				Generalized-MLI				Proposed MLI			
Levels→	*3*	*5*	*7*	*9*	*3*	*5*	*7*	*9*	*3*	*5*	*7*	*9*	*3*	*5*	*7*	*9*	*3*	*5*	*7*	*9*
Parameters↓																				
No. of *dc* voltage source	1	2	3	4	1	1	1	1	1	1	1	1	1	1	1	1	1	2	3	4
No. of switches	4	8	12	16	4	8	12	16	4	8	12	16	6	10	16	24	5	6	7	8
No. of diodes	–	–	–	–	–	–	–	–	1	6	15	28	–	–	–	–	1	3	6	10
No. of capacitor	–	–	–	–	3	10	21	36	2	4	6	8	1	3	6	10	–	–	–	–
Total count	**4**	**8**	**12**	**16**	**7**	**18**	**33**	**52**	**7**	**18**	**33**	**52**	**7**	**13**	**22**	**30**	**6**	**9**	**13**	**18**

Fig. 4 shows the constructional power circuit of proposed MLI topology for 7–level output voltage. This 7–level MLI consists of three *dc* voltage sources each having the magnitude of V_{dc}, three switches (termed as Group – I switches) as a part of the power structure for generating 4–level unidirectional stepped voltage waveform, and four switches (termed as Group – II switches) as a part of the H–bridge inverter for converting the 4–level unidirectional stepped voltage into 7–level bidirectional voltage at the load terminals. Moreover, the proposed 7–level MLI topology also comprises of six diodes. Here, switches of Group–I determine the unidirectional input voltage to the H-bridge, whereas switches of Group–II have the sole purpose of conversion of the unidirectional input voltage, V_{AB}, into bidirectional output voltage, V_{XY}. V_{XY} and V_{AB} have equal peak magnitudes; however switching state of Group–II switches decides the polarity of load voltage.

Switching states for 7–level proposed MLI topology and the corresponding output voltages are provided in Table II. Switching states 4 and 7 produce the peak value of V_{AB} (=3V_{dc}). The switches of Group-I, S_{p1}-S_{p3}, conduct during these states. The current during the state 4 follows the path: P4-V_{dc}-V_{dc}-V_{dc}-P1-S_{p1}-S_{p2}-S_{p3}-A-S_{b1}-X-load-Y-S_{b2}-P4.

Complementary of the switching states 4 and 7, i.e. state 1, results in zero voltage across the terminals A and B. The current circulates in the H–bridge circuit in this state through previously ON switch either S_{b1}-S_{b2} or S_{b3}-S_{b4} and diode D_{3c}. For, V_{AB}=2V_{dc}, switching state 3 and 6 have to be activated. Current flow during these states is facilitated by turning ON S_{p2} and S_{p3}.

After activation of state 3, the current will follow the path: P4-V_{dc}-V_{dc}-P2-D_{1a}-S_{p2}-S_{p3}-A-S_{b1}-X-load-Y-S_{b2}-B-P4. For switching state 2 and 5, V_{AB} equals V_{dc}. In these states only S_{p3} will be conducting and allows the current to flow through load from lower *dc* voltage source, V_{dc}. However switching state of S_{b1} to S_{b4} determines the polarity of V_{XY}. The current path for switching state-2 is P4-V_{dc}-P3-D_{2b}-S_{p3}-A-S_{b1}-X-load-Y-S_{b2}-B-P4.

TABLE II. SWITCHING TABLE OF PROPOSED 7-LEVEL MLI

State	V_{AB}	S_{p1}	S_{p2}	S_{p3}	S_{b1} & S_{b2}	S_{b3} & S_{b4}	V_{XY}
1	**0**	0	0	0	1	0	**0**
2	V_{dc}	0	0	1	1	0	$+V_{dc}$
3	$2V_{dc}$	0	1	1	1	0	$+2V_{dc}$
4	$3V_{dc}$	1	1	1	1	0	$+3V_{dc}$
5	V_{dc}	0	0	1	0	1	$-V_{dc}$
6	$2V_{dc}$	0	1	1	0	1	$-2V_{dc}$
7	$3V_{dc}$	1	1	1	0	1	$-3V_{dc}$

IV. CALCULATION OF LOSSES

Power electronic switches suffer encounter conduction and switching losses during their operation. Conduction loss occurs when power switches in conduction state. They come into the picture because of the internal resistance of the switch. These losses depend on the on state voltage drop and current flowing through the switch. Switching losses encountered when the switch turn ON and OFF. These losses represent the energy consumed in turning the switch ON or OFF. They depend on the switching frequency. Higher the switching frequency, higher will be the switching losses.

A. Conduction losses

Conduction loss depends on duty cycle as it caused in the converter when power switches are in the ON state. Switch and diode conduction losses are one of the major losses in power supply. Conduction loss for typical switch and diode are calculated using equations specified in (4) and (5), respectively [3].

$$P_{CLSW}(t) = I_{rms}^2(t) \times R_{\text{int}} \tag{4}$$

$$P_{CLD}(t) = V_D \times I_{DAVG}(t) \tag{5}$$

where, P_{CLSW} is conduction loss of the switches, P_{CLD} is the conduction loss in diodes, I_{rms} is the RMS value of the switch current, R_{int} is the internal equivalent resistance of the respective switch, V_D is diode forward voltage drop and I_{DAVG} is average current flowing through diode. The current flowing through power switches and diodes depends on the output voltage level. For the proposed MLI topology, the current flows through one diode and two, three, four, five switches for V_{XY}= zero, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ respectively. For 7–level output voltage, total conduction loss for half cycle can be calculated by (6).

$$P_{CL_T}(t) = \sum_{i=0}^{3} P_{CLD_j}(t) + (i+2) \times P_{CLSW_j}(t) \tag{6}$$

where, P_{CL_T} is total conduction loss faced by 7–level MLI topology during one half cycle, i indicates particular switching state (i.e. output voltage level) which again depends on the time during the respective half cycle, for instance, i=0, 1, 2, 3 indicates switching state 1, 2, 3 and 4 respectively of respective positive half cycle and j indicates the respective IGBT/ diode in the conduction state.

B. Switching losses

When a power semiconductor switch turns ON or OFF, switching loss occurs. Number of turn ON and OFF to which the switch is subjected to for a given time, depends on the switching frequency. As the inverter switches are operated at high switching frequency, switching loss forms a major part of inverter losses. Switching losses for a power semiconductor switch and diode, [21], can be expressed as,

$$P_{SLSW}(t) = f_{sw} \times (E_{I_{ON}} + E_{I_{OFF}}) \tag{7}$$

$$P_{SLD}(t) = f_{sw} \times (E_{D_{ON}} + E_{D_{OFF}}) \tag{8}$$

where, P_{SLSW} is switching loss of the switches, P_{SLD} is the switching loss in diode, f_{sw} is the switching frequency of the respective power electronic converter, $E_{I_{ON}}$ and $E_{I_{OFF}}$ are the energy loss occurring in the switch during turning ON and OFF, and $E_{D_{ON}}$ and $E_{D_{OFF}}$ are the energy loss occurring in the diodes during turning ON and OFF. The proposed 7–level MLI topology, shown in Fig. 4, comprises of seven IGBTs and six diodes. Depending on the level of output voltage, the IGBT/s and diode/s that conduct are listed in Table II. The total switching loss for the proposed 7–level MLI topology can be given as,

$$P_{SL_T}(t) = \sum_{i=0}^{3} P_{SLD_j} + (i+2) \times P_{SLSW\,j} \tag{9}$$

where, P_{SL_T} is the total switching loss occurs in the proposed 7–level MLI topology for respective half cycle. The total losses occurring in the proposed 7–levlel MLI can be determined as,

$$P_{loss_T}(t) = P_{CL_T}(t) + P_{SL_T}(t) \tag{10}$$

where, P_{loss_T} is the total loss of the proposed 7–level MLI topology.

V. Proposed 7–Level MLI Based MVD

The proposed 7–Level MLI is employed as a part of MVD for driving a 3–phase induction motor. As 3–phase *ac* supply is required to drive the 3–phase induction motor, three proposed 7–level MLIs are separately employed to control the power being delivered to each of the three phases of the induction motor.

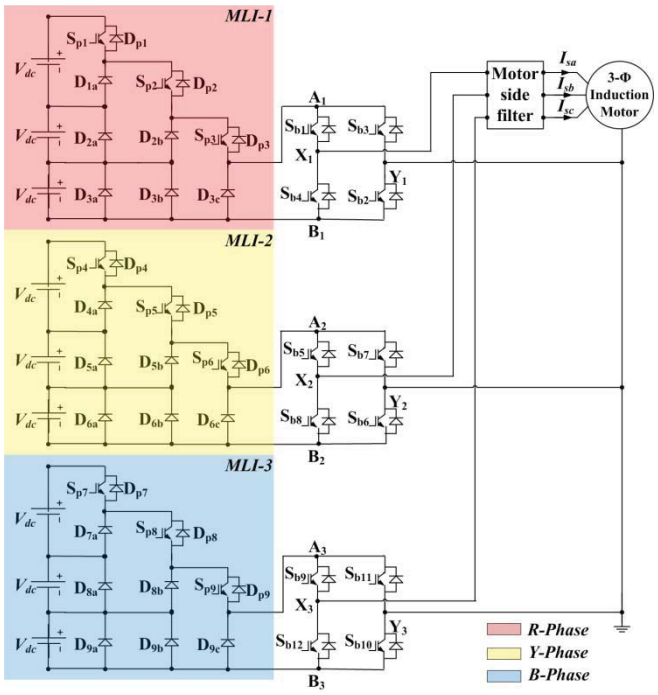

Fig. 5. Proposed 7–level MLI based MVD feeding a 3–phase induction motor

Fig. 5 shows the three separate MLI topologies feeding individual phases of induction motor where S_{p1}-S_{p3}/D_{p1}-D_{p3}, S_{p4}-S_{p6}/D_{p4}-D_{p6}, S_{p7}-S_{p9}/D_{p7}-D_{p9} are the IGBTs/diodes of Group-I of the respective phases, S_{b1}-S_{b4}/D_{b1}-D_{b4}, S_{b5}-S_{p8}/D_{p5}-D_{p8}, S_{p9}-S_{p12}/D_{p9}-D_{p12} are the IGBTs/diodes of Group–II of the respective phases, V_{dc} is the input *dc* source that is having equal magnitude for all three MLI topologies and I_{sa}, I_{sb}, I_{sc} are the three phase stator current fed by the set of three proposed 7–level MLI topology. From Fig. 5, it is observed that the three phases from points X_1, X_2 and X_3 feeds the three phases of the induction motor and from point Y_1, Y_2 and Y_3, the phases are connected to the neutral of the induction motor. This system, shown in Fig. 5, is modeled in PSIM software platform. Pulse width modulation (PWM) method is considered in the 7–level MLI topology.

VI. Results

Simulation study is carried out for the proposed 7–level MLI topology based 3–phase induction motor drive. The scope of this work is focused on simulation and analysis of the proposed 7–level MLI topology driving induction motor. The specifications of switches and induction motor to be used in prototype MVD are considered in simulation studies and the same is given in Appendix. The control of speed of the induction motor is ensured by implementing scalar method. However, this can also be extended to field oriented control. As the control strategy is related to the generation of three reference voltages, which are used to control the switching of MLI, the change of control strategy does not affect the working of MLI. The simulation results of prototype MVD, comprising of the proposed 7–level MLI feeding a 3–phase induction motor, are shown in Fig. 6–12.

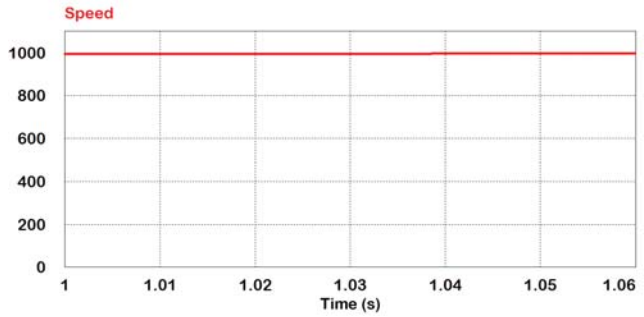

Fig. 6. Steady state rotor speed

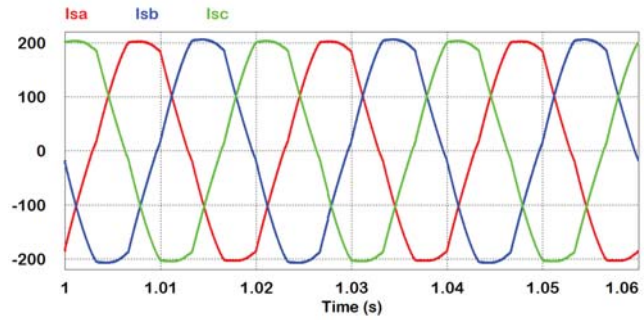

Fig. 7. Stator currents

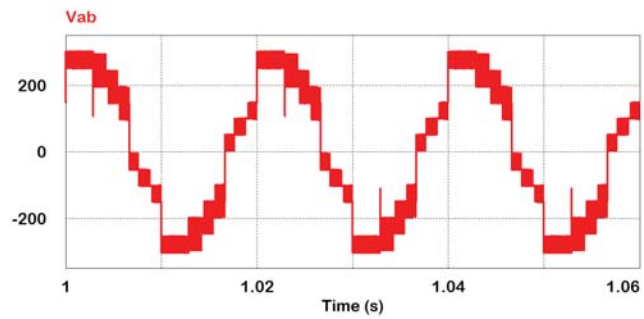

Fig. 8. Line voltage occurred across stator winding

Each MLI unit feeds an individual phase of the motor. The MLI unit is controlled to generate the phase voltage such that sinusoidal currents are drawn by the respective stator winding so that the steady state rotor speed is achieved. Fig. 6 shows the steady state rotor speed of the 3–phase induction motor. The steady state rotor speed is 1000 RPM and the peak-to-peak ripple is 1 RPM. The 3–phase stator currents, I_{sa}, I_{sb} and I_{sc}, shown in Fig. 7, are sinusoidal with the peak amplitude of 202.8 A and THD of 3.9% which adheres to the limit set by the IEEE standard 1566-2015 [22]. Fig. 8 shows the line voltage, V_{ab}.

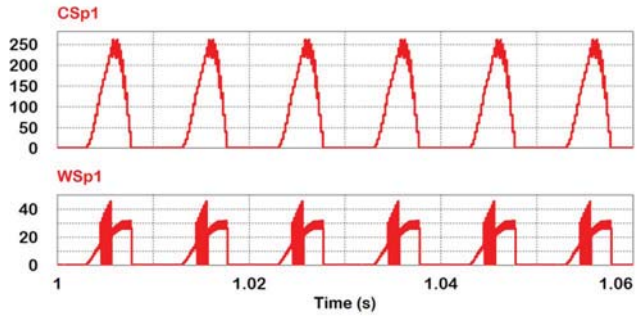

Fig. 9. Conduction and switching loss of switch S_{p1}

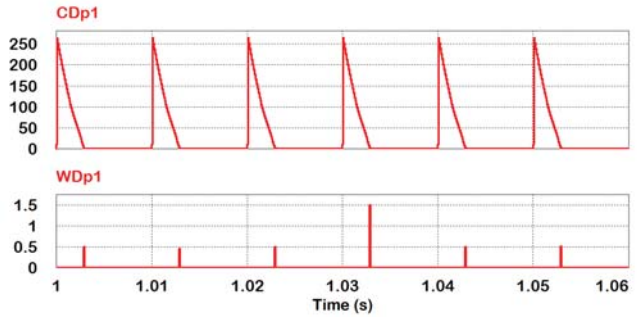

Fig. 10. Conduction and switching loss of diode D_{p1}

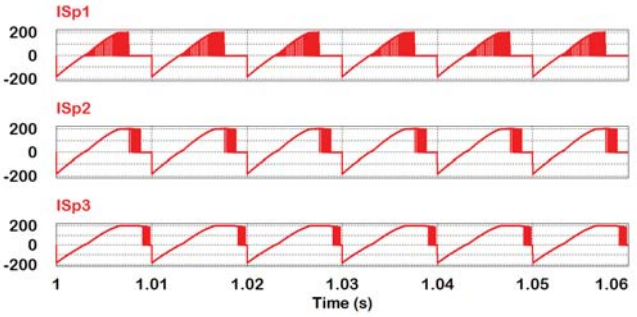

Fig. 11. Current flowing through switches S_{p1}, S_{p2} and S_{p3}

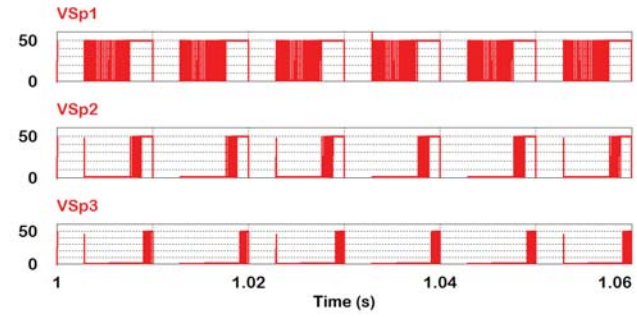

Fig. 12. Voltage encountered by switches S_{p1}, S_{p2} and S_{p3}

With each MLI unit catering to the individual phase, V_{ab} has the peak value of 302 V and THD of 21.8%. The conduction and switching loss of the IGBT switch S_{p1}, respectively denoted as C_{Sp1} and W_{Sp1}, are shown in Fig. 9. From Table II, it is clear that S_{p1} conducts during switching state 4 and 7. During these states, switch S_{p1} is subjected to the gate pulses generated through PWM. Based on the reference and the carrier signal, the ON and OFF period of

the switch is determined. From Fig. 9, it is also observed that conduction loss and switching loss occurs when switching state 4 and 7 is activated. In the same way conduction and switching loss for the body diode D_{p1}, respectively denoted as C_{Dp1} and W_{Dp1}, of switch S_{p1} is shown in the Fig. 10. Fig. 11 shows the currents I_{sp1}, I_{sp2}, I_{sp3}, flowing through the switches S_{p1}, S_{p2} and S_{p3}. S_{p1} is supposed to be ON for state 4 and 7, whereas S_{p2} is ON for states 3, 4, 6 and 7. However S_{p3} is supposed to be ON for all states, except state 1 when the zero output voltage is generated. During the states, when the switch is supposed to be ON, it is subjected to PWM gate pulses so as to control the current and achieve desired speed. The voltage encountered by these switches, V_{sp1}, V_{sp2} and V_{sp3}, during the operation of MLI are shown in Fig. 12. The peak voltages appearing across S_{p1}, S_{p2} and S_{p3} are 50 V. The ON state voltages for across S_{p1}, S_{p2} and S_{p3} are 1.45 V, 1.6 V and 1.65 V respectively. From these results shown in Fig. 6-12, it is clear that the proposed 7-level MLI topology generates stepped voltage waveform which results in sinusoidal stator currents and the magnitude of these currents can be controlled to control the speed of induction motor. With switch count being lower than the three basic and the generalized MLI topologies, the proposed topology would be ideal for the MVDs.

VII. Conclusion

In this work a reduced switch symmetrical MLI topology is proposed and its operation for a MVD feeding a 3–phase induction motor is analyzed by considering three separate sets of proposed MLI units for each of the three phases of stator winding. With the employment of the proposed MLI for MVD application, the benefits of reduction in filter size, lower *dv/dt* and voltage stresses for the power semiconductor switches and ease operation for high power application, etc. can be derived. With the help of the standard control strategies for induction motors, the proposed 7–level MLI topology in the MVD can ensure sinusoidal stator currents with THD less than 5% and reduced stator voltage distortions. This can further help in reducing speed and torque ripple leading to improved drive operation. The proposed symmetrical MLI topology further derives the benefits of good modularity, simple modulation and control. The reduced component count in the proposed MLI topology ensures the reduction in the switching and conduction loss. Moreover, it leads to less complexity in the control strategy, lesser gate drive requirements and reduced protection units.

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Appendix

Specification:

Induction motor: Stator resistance (R_s)=0.289 Ω, Rotor resistance (R_r)= 0.153 Ω, Stator inductance (L_s)=1.3mH, Rotor inductance (L_r)= 0.7 mH, Mutual inductance (L_m)=1 mH.

IGBT: Powerex CM1000HA-24H, $V_{ce(max)}$=1200 V, $I_{c(max)}$= 1000 A.